

FIG. 1

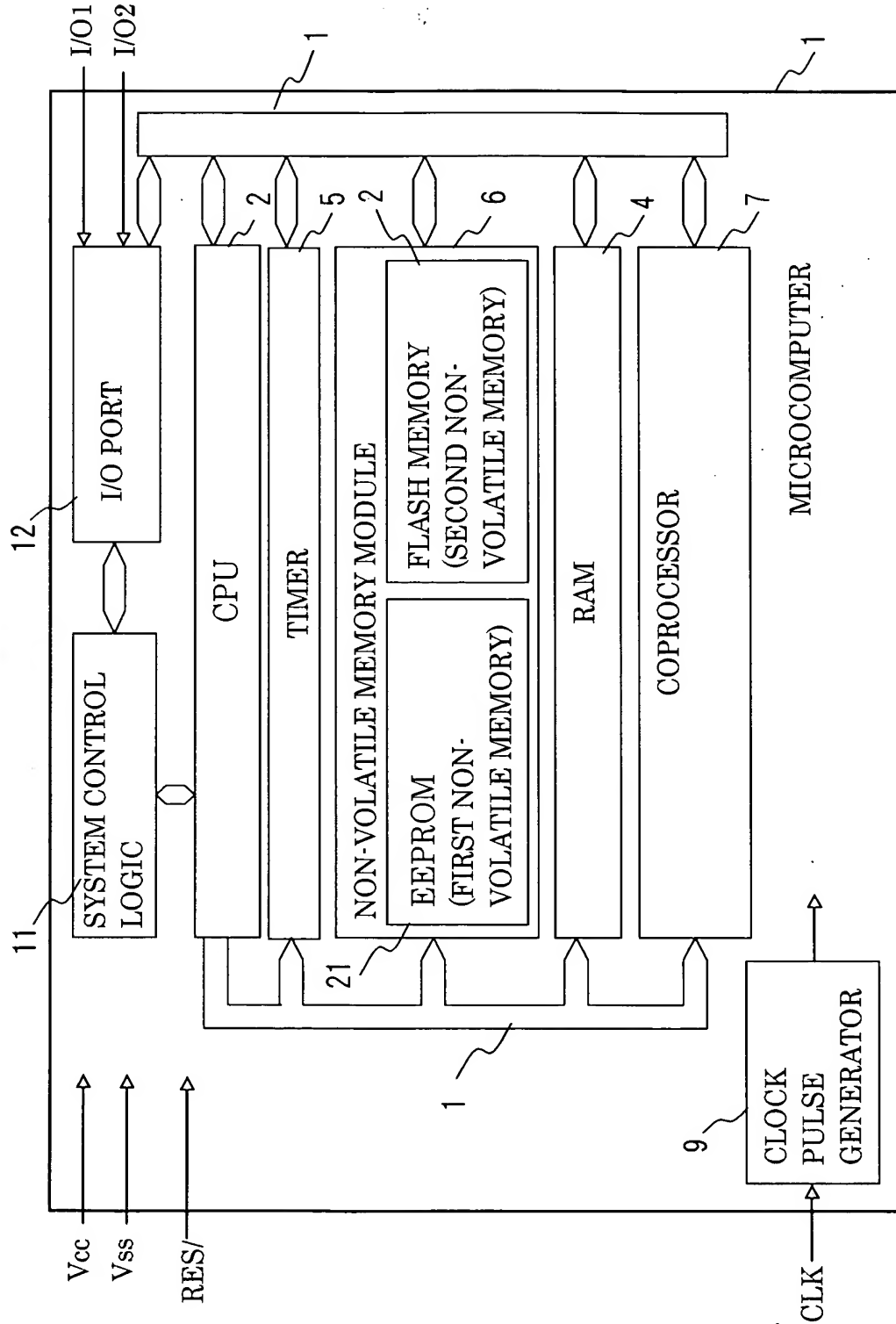


FIG. 2

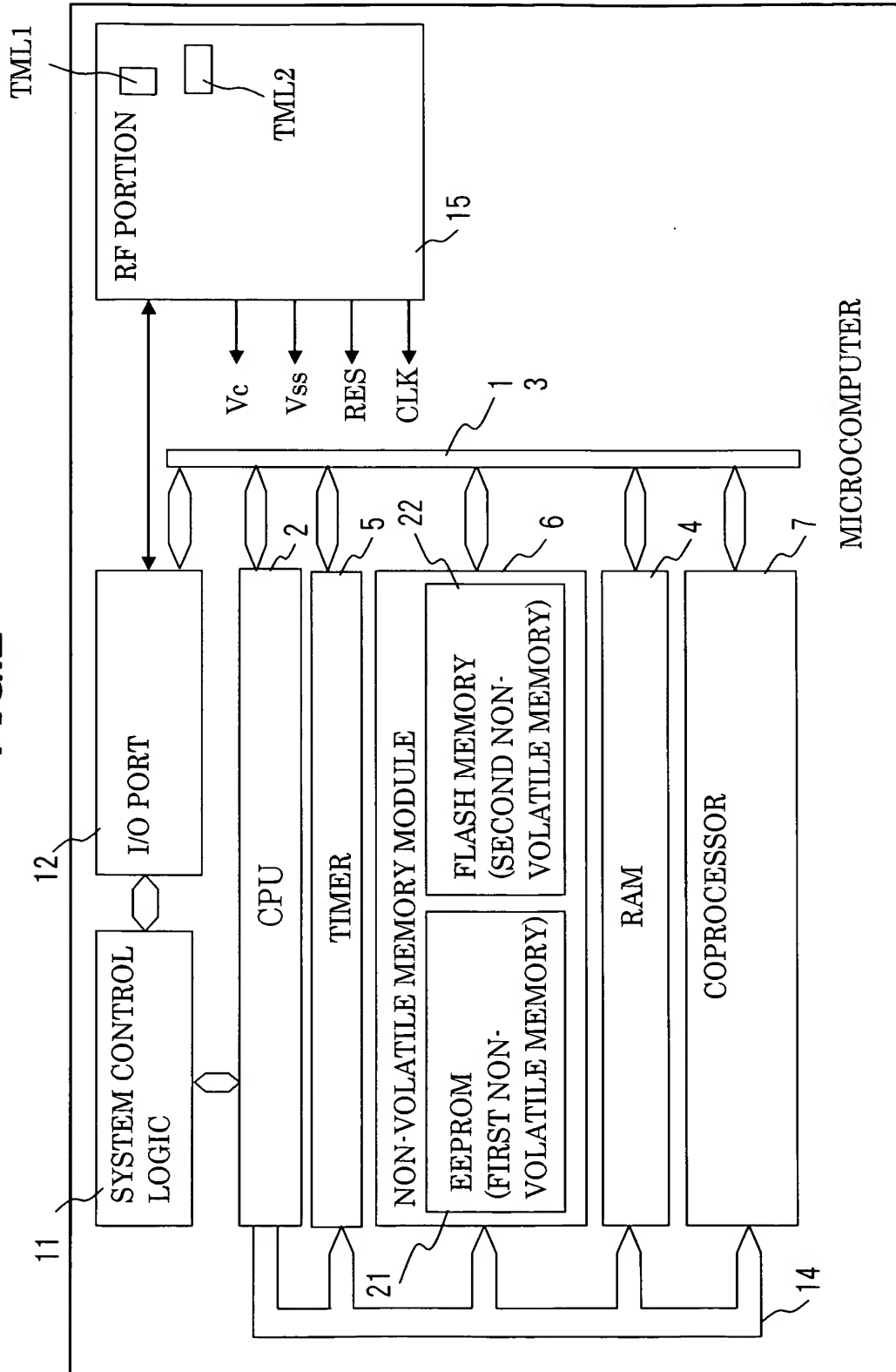


FIG. 3

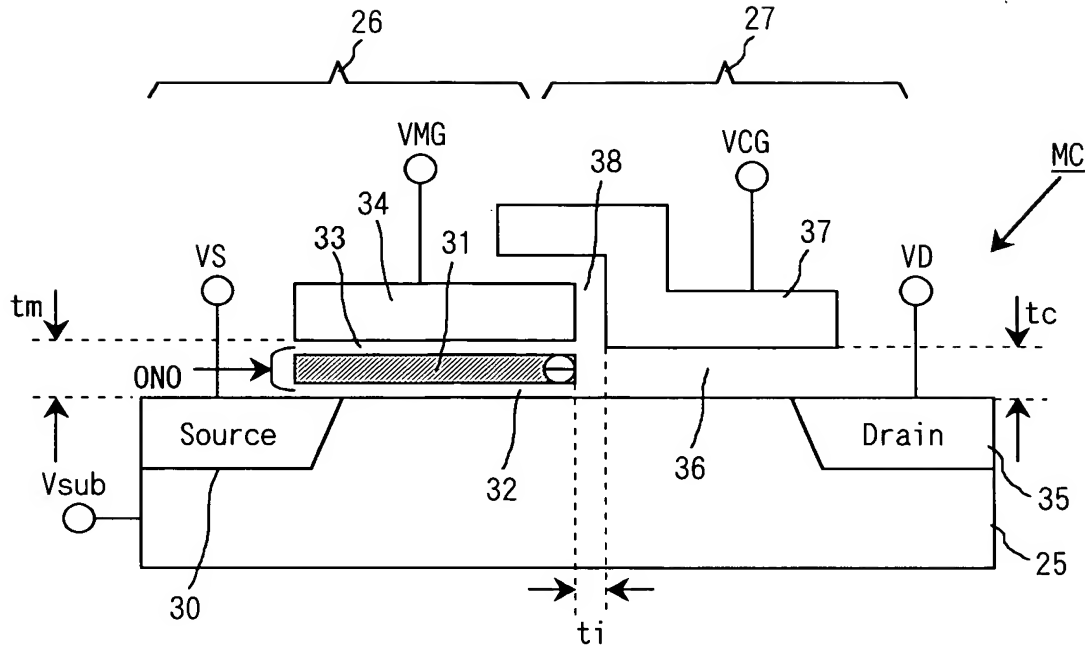


FIG. 4

	VD	VCG	VMG	VS	Vsub
Read	1.5V	1.5V	0V	0V	0V
Write	0.5V	1.5V	10V	6V	0V
Erase	0V	1.5V	12V	0V	0V

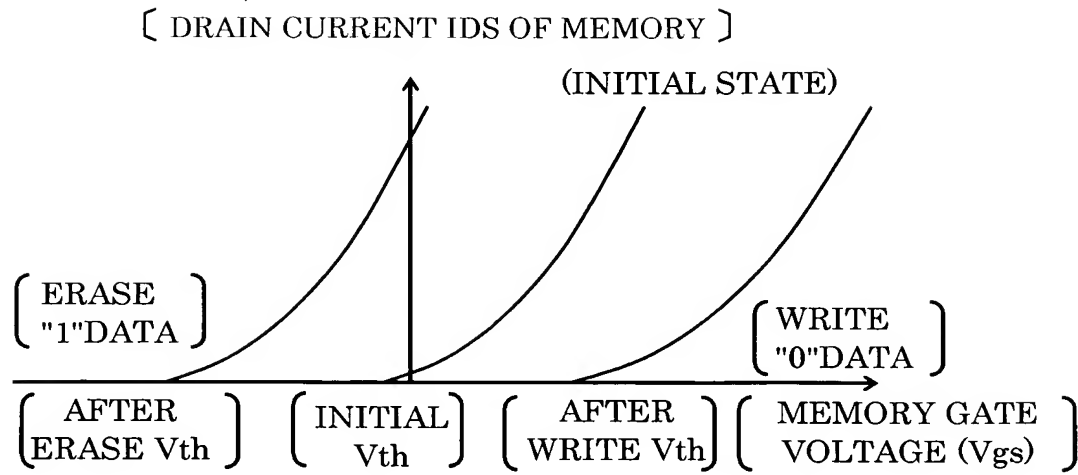
FIG.5

FIG. 6

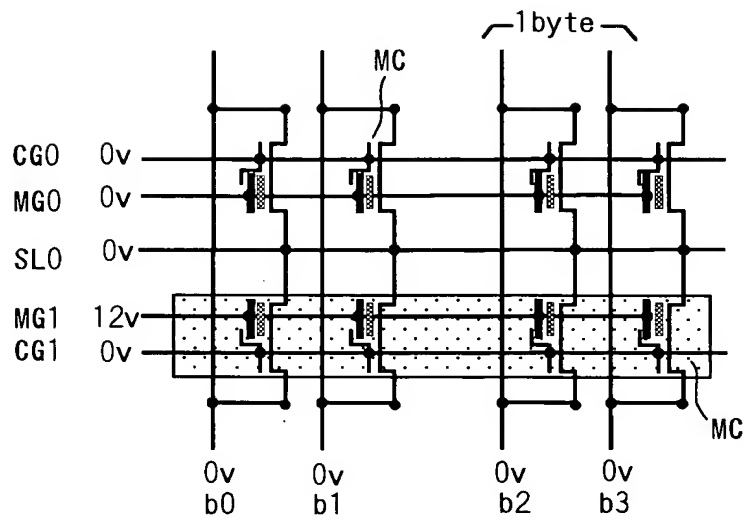


FIG. 7

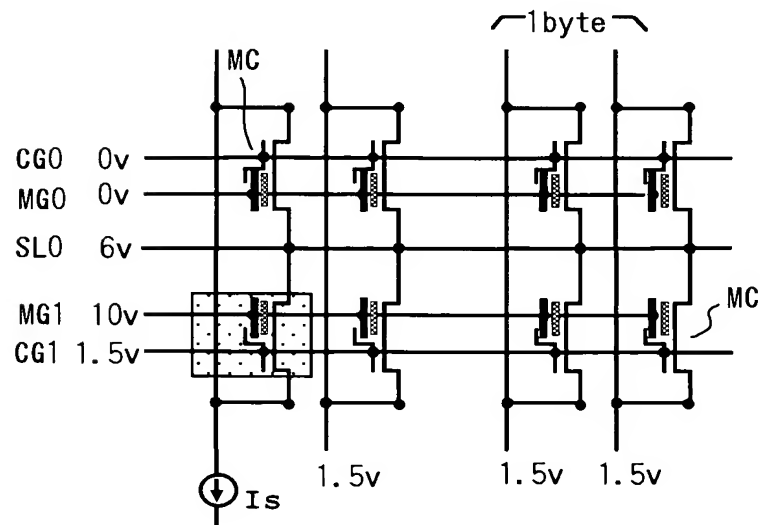


FIG. 8

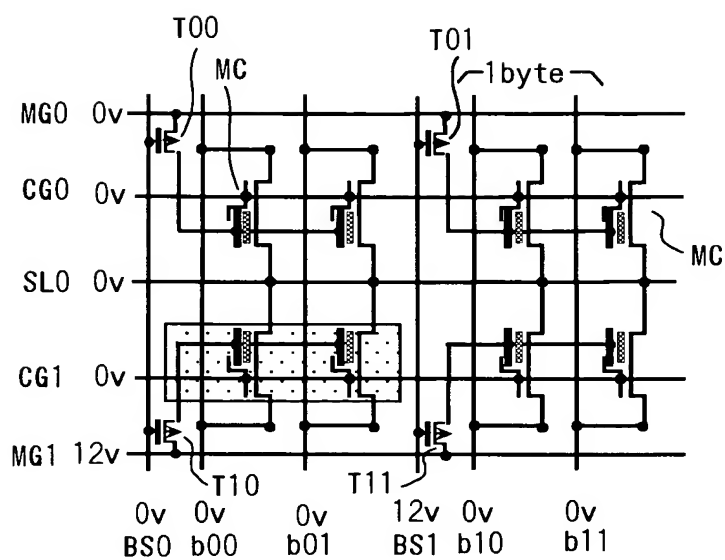


FIG. 9

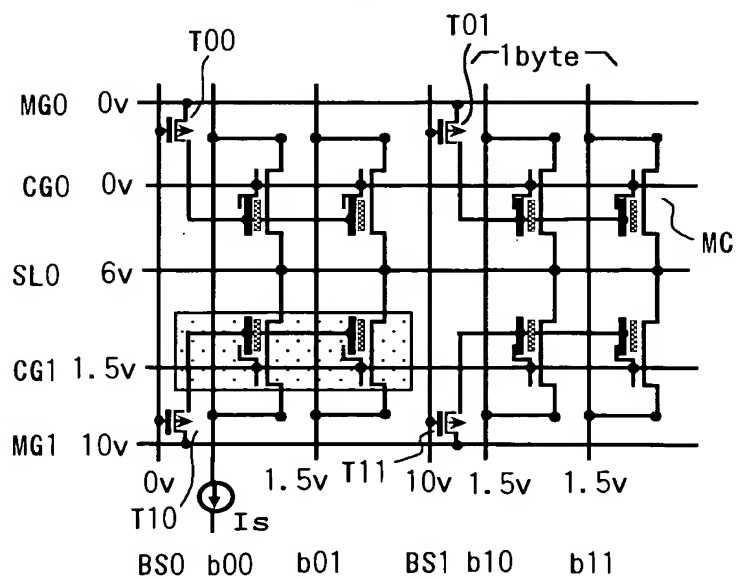


FIG. 10

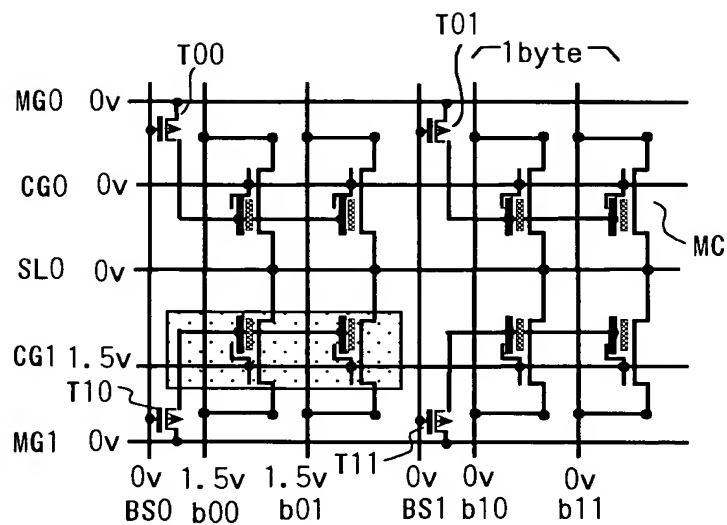


FIG. 13

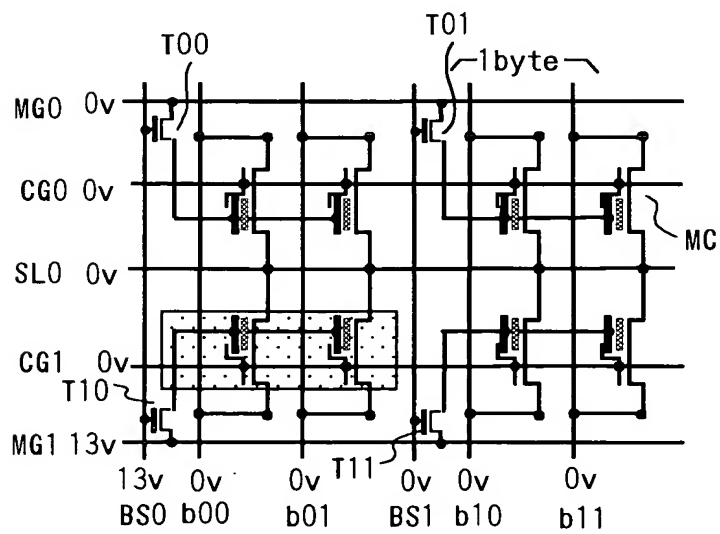


FIG. 11

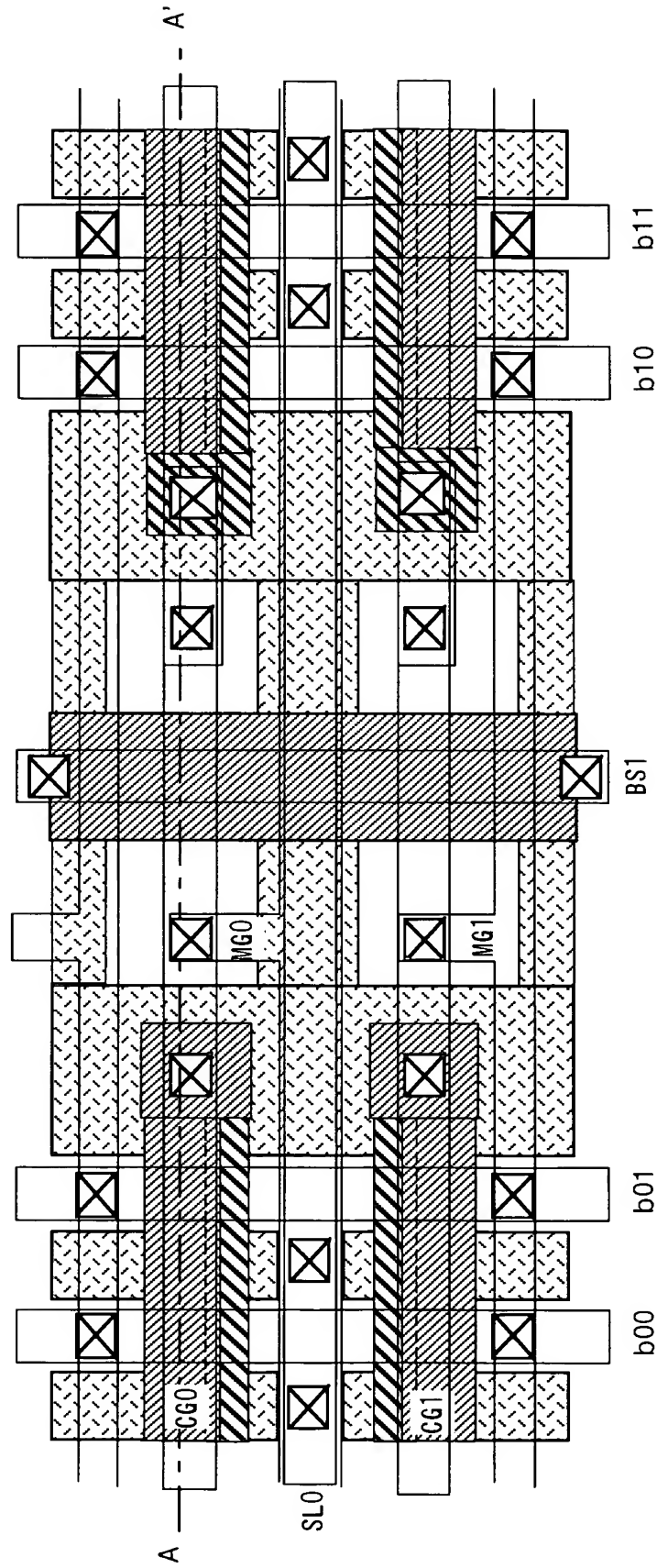


FIG. 12

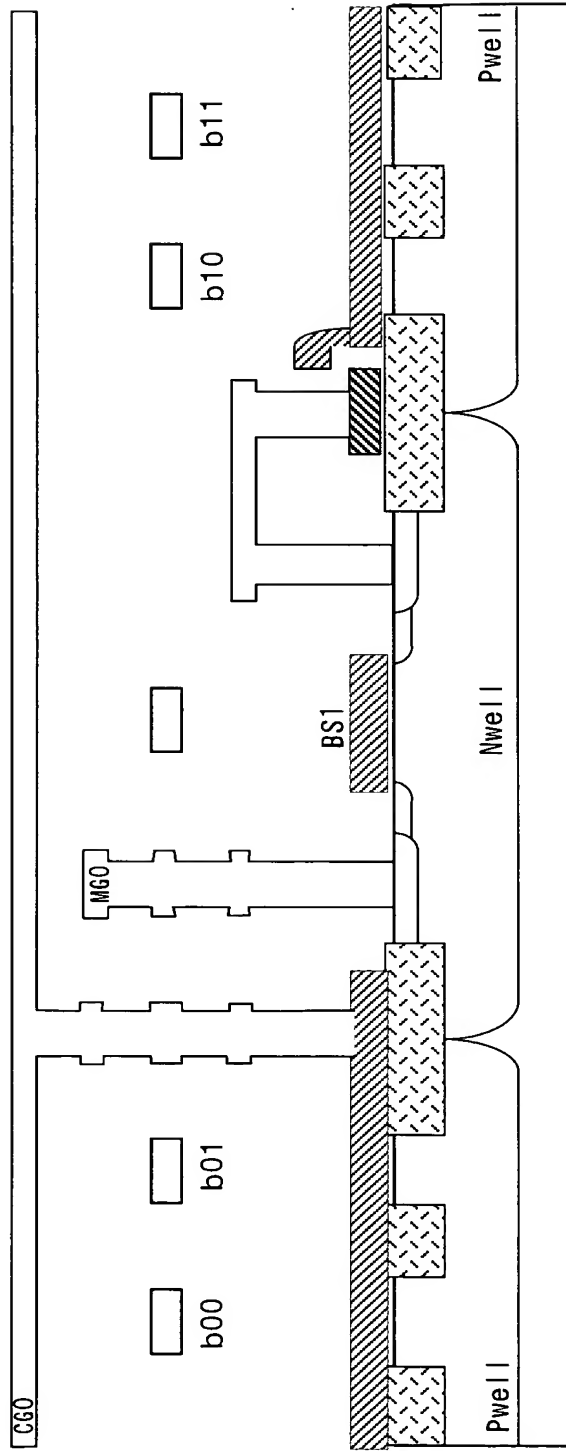


FIG. 14

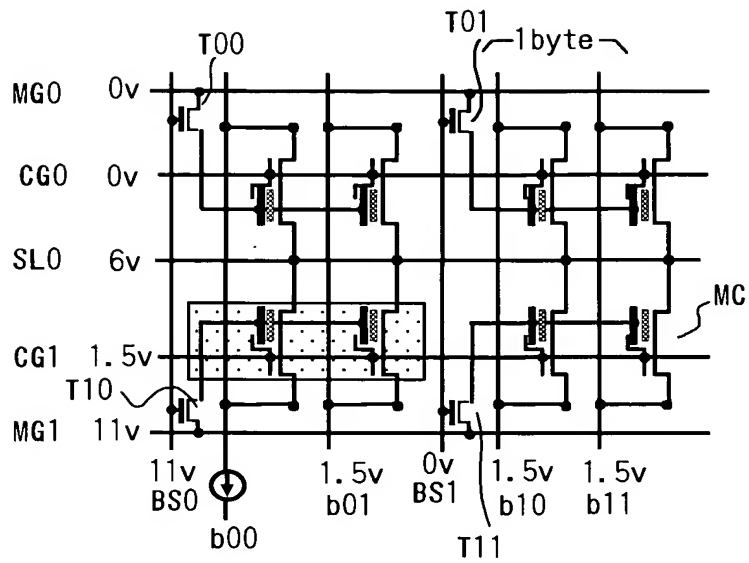


FIG. 15

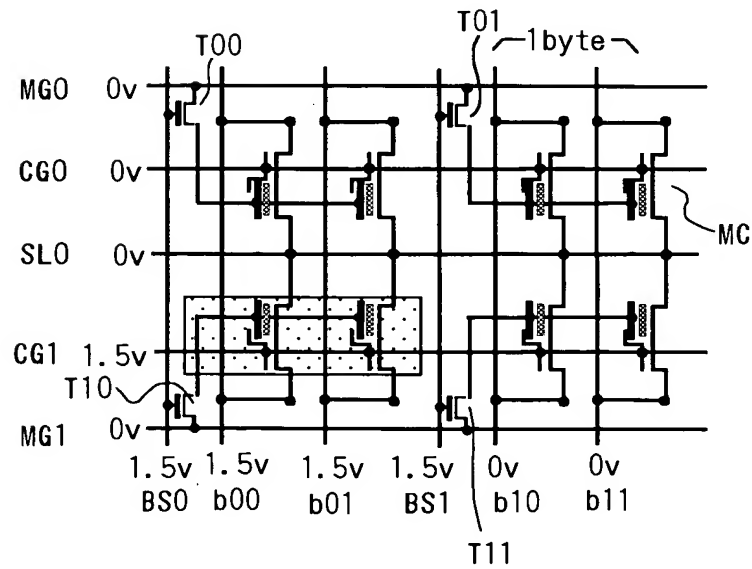


FIG. 16

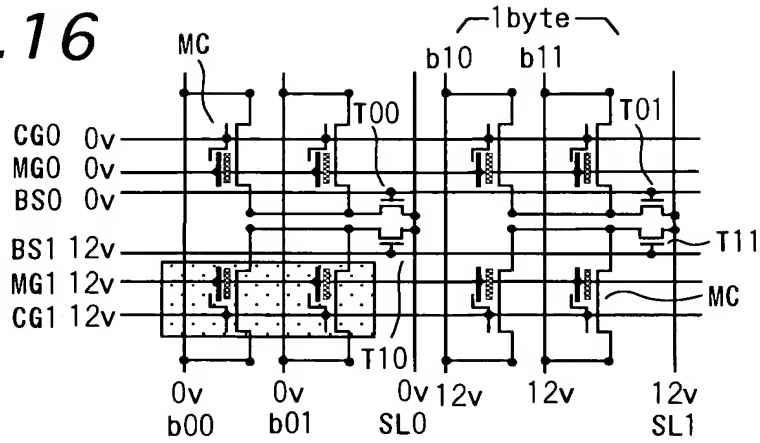


FIG. 17

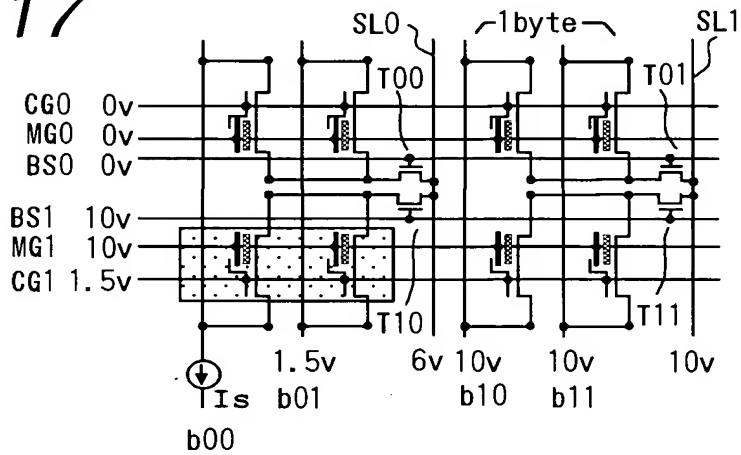


FIG. 18

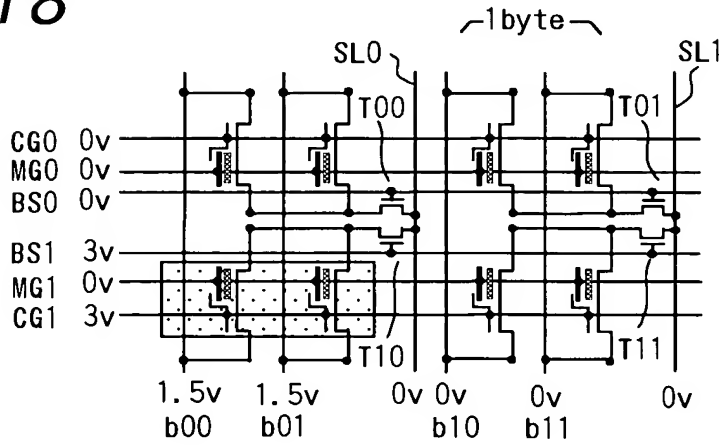


FIG. 19

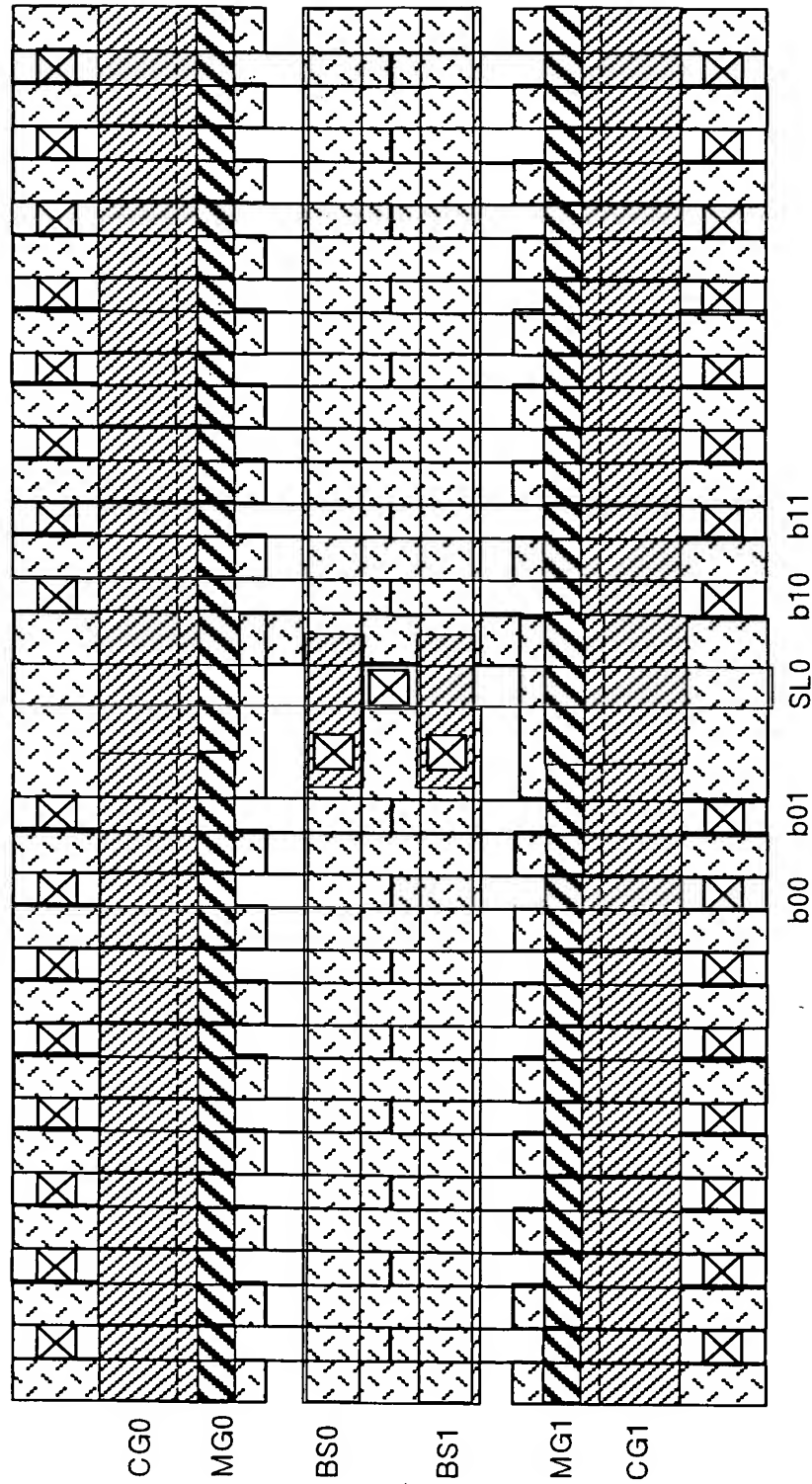


FIG. 20

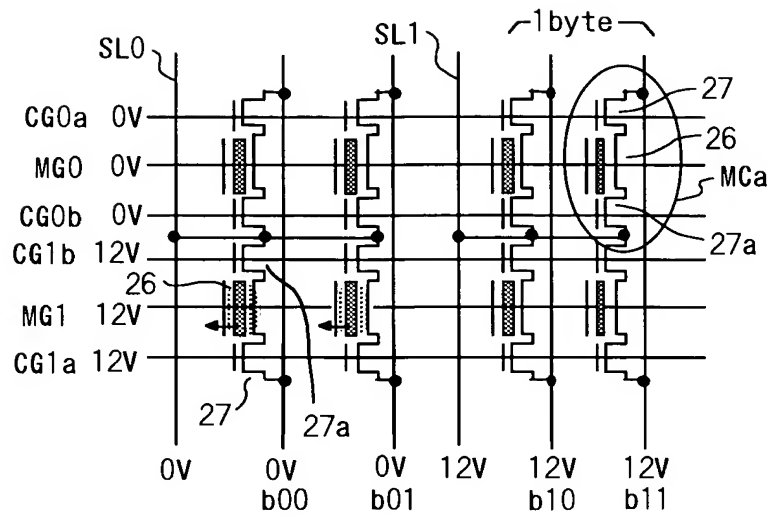


FIG. 21

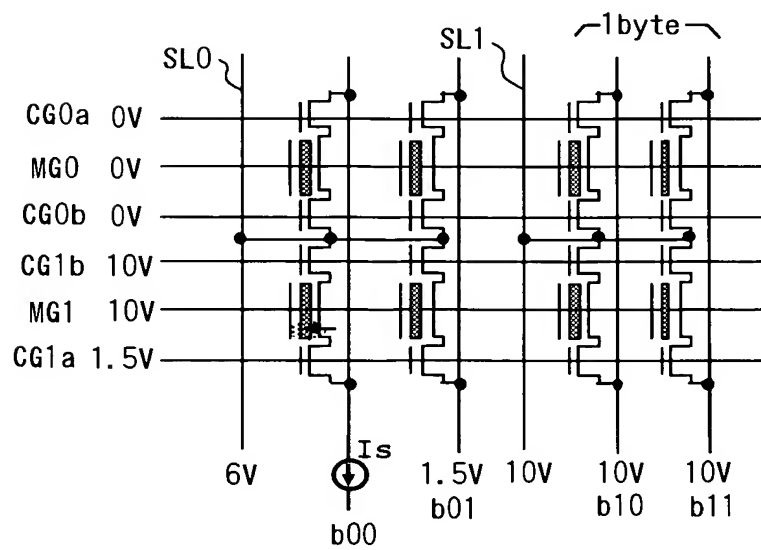


FIG.22

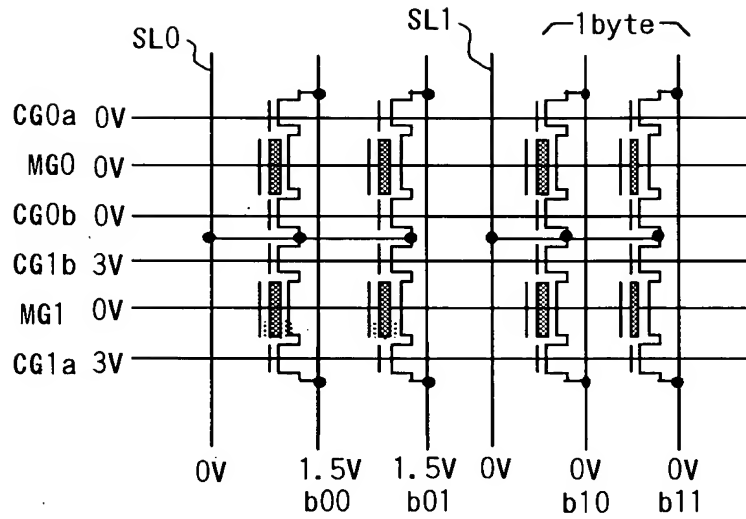


FIG.23

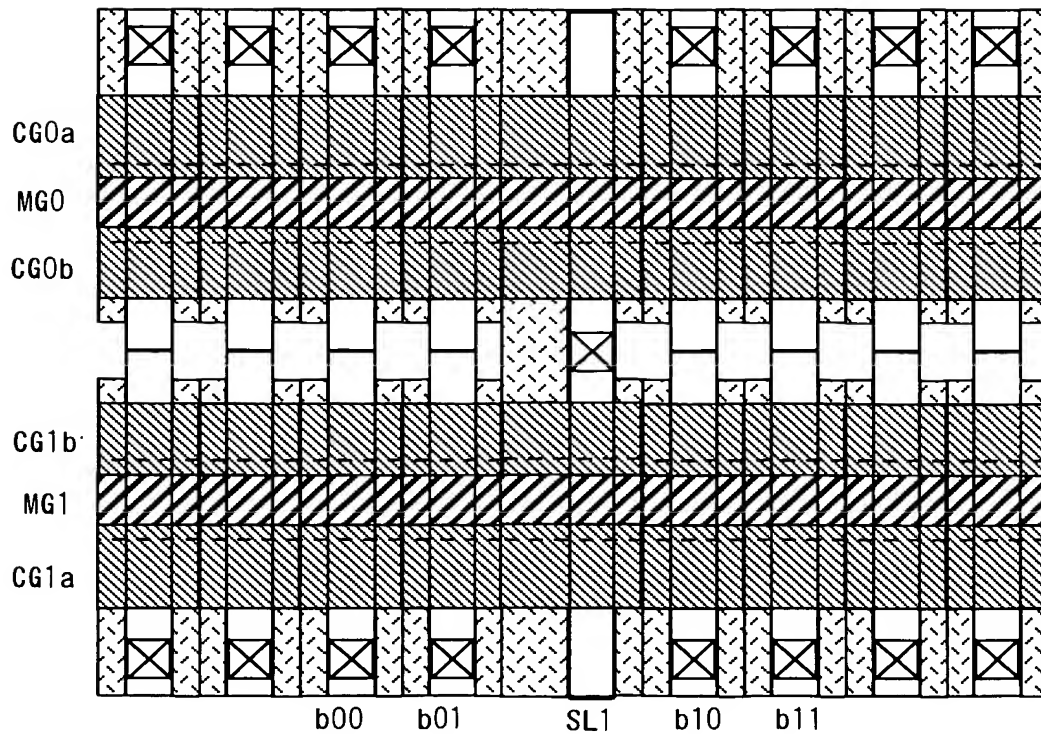


FIG. 24

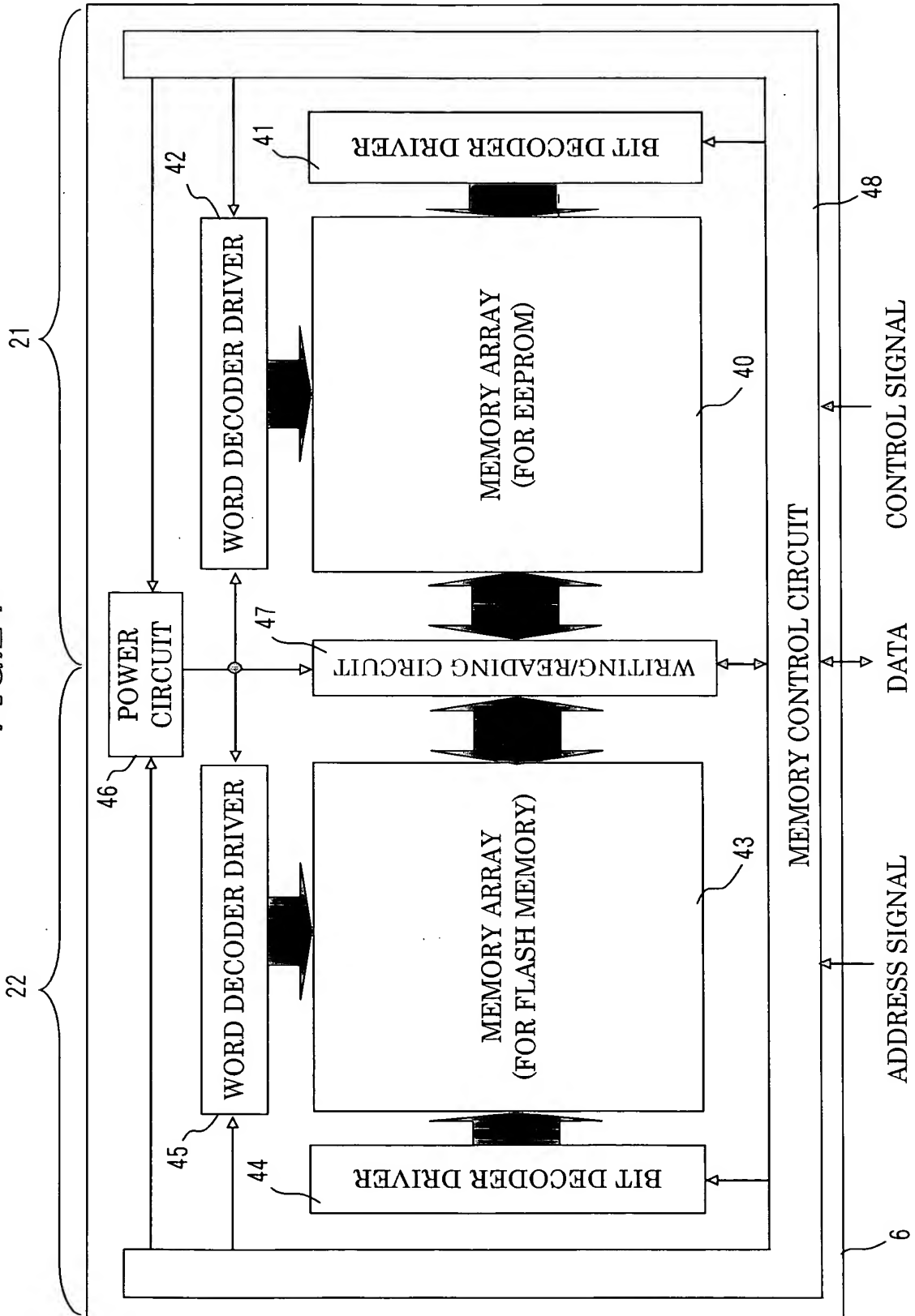


FIG. 25

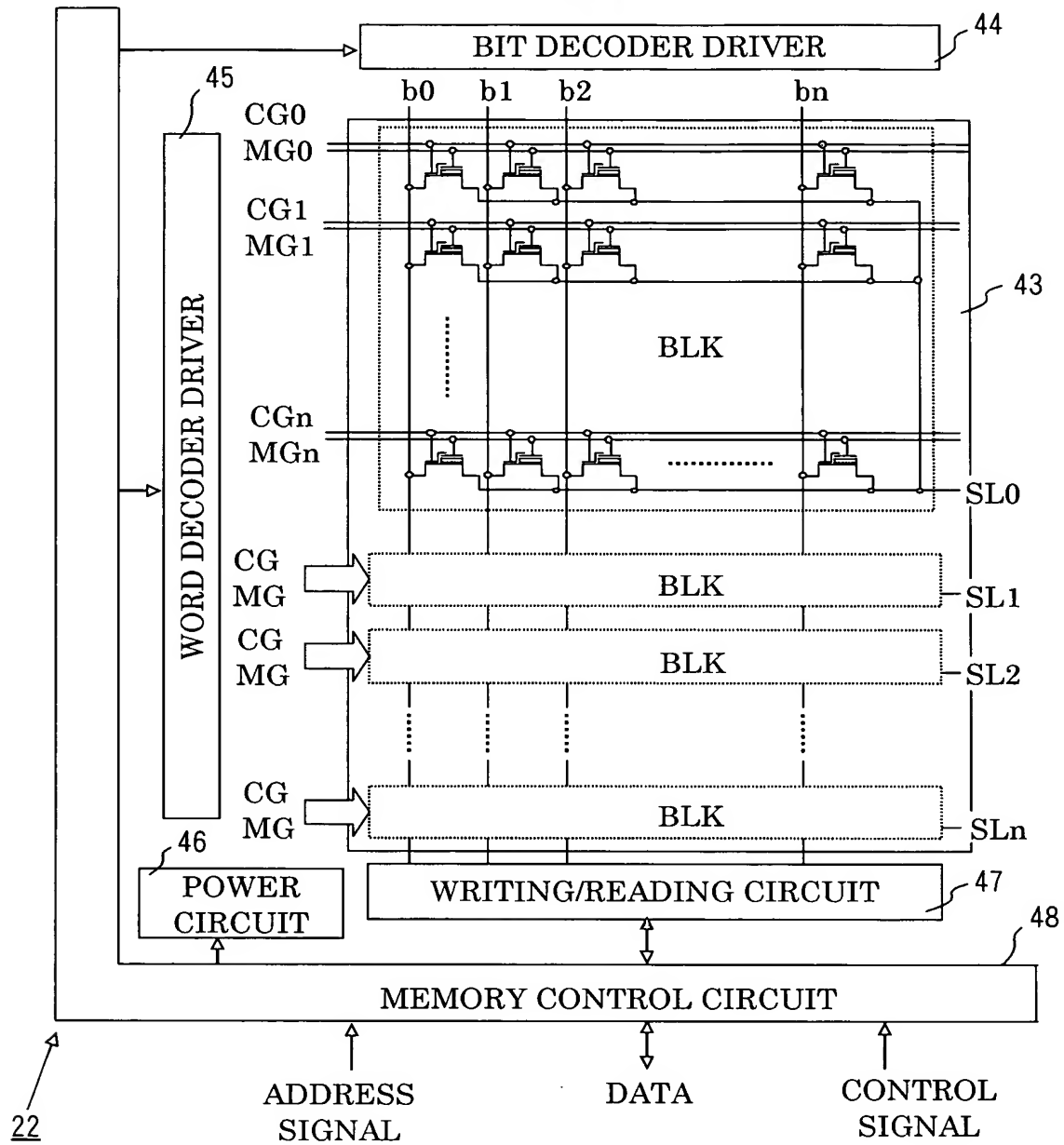


FIG. 26

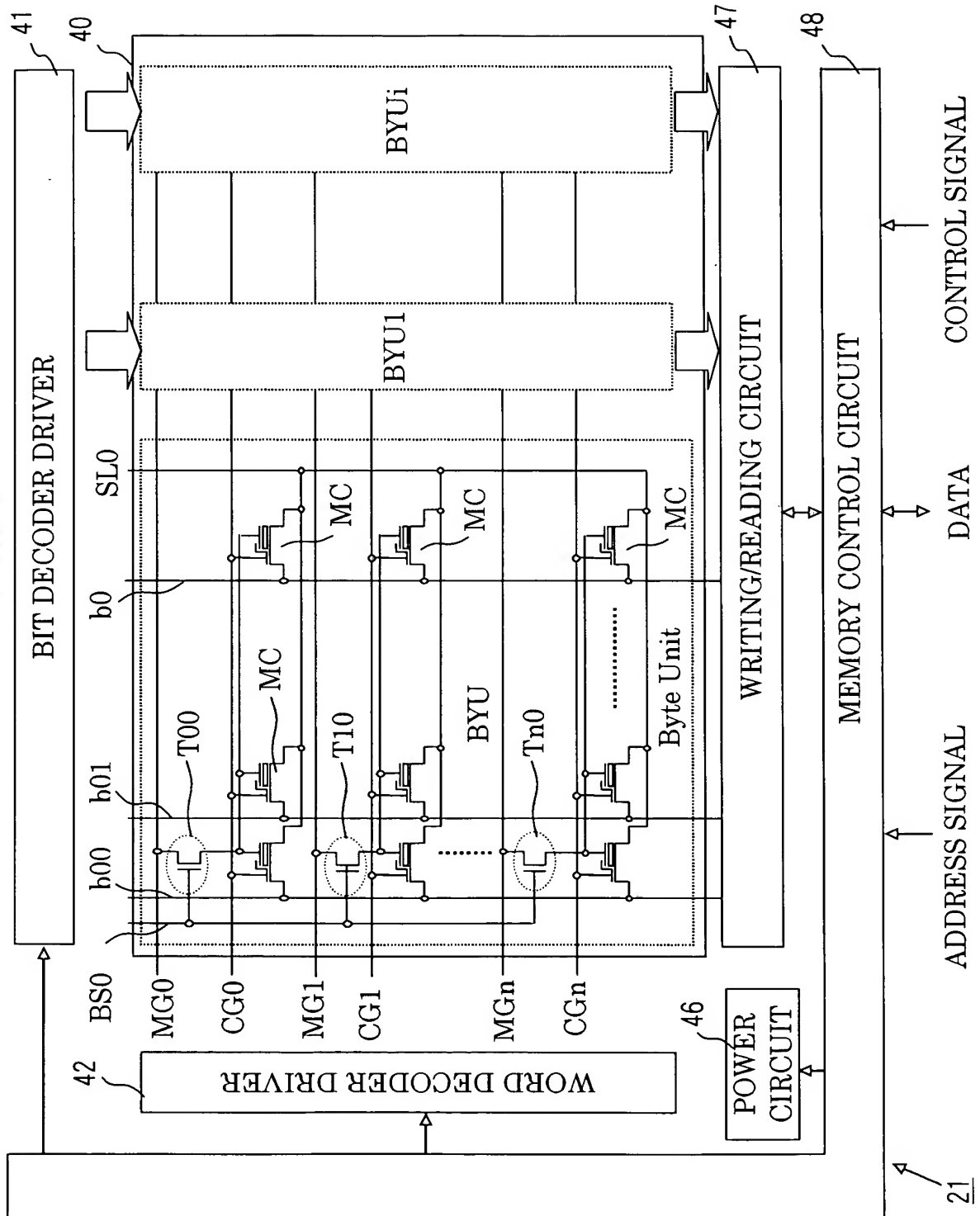


FIG. 27

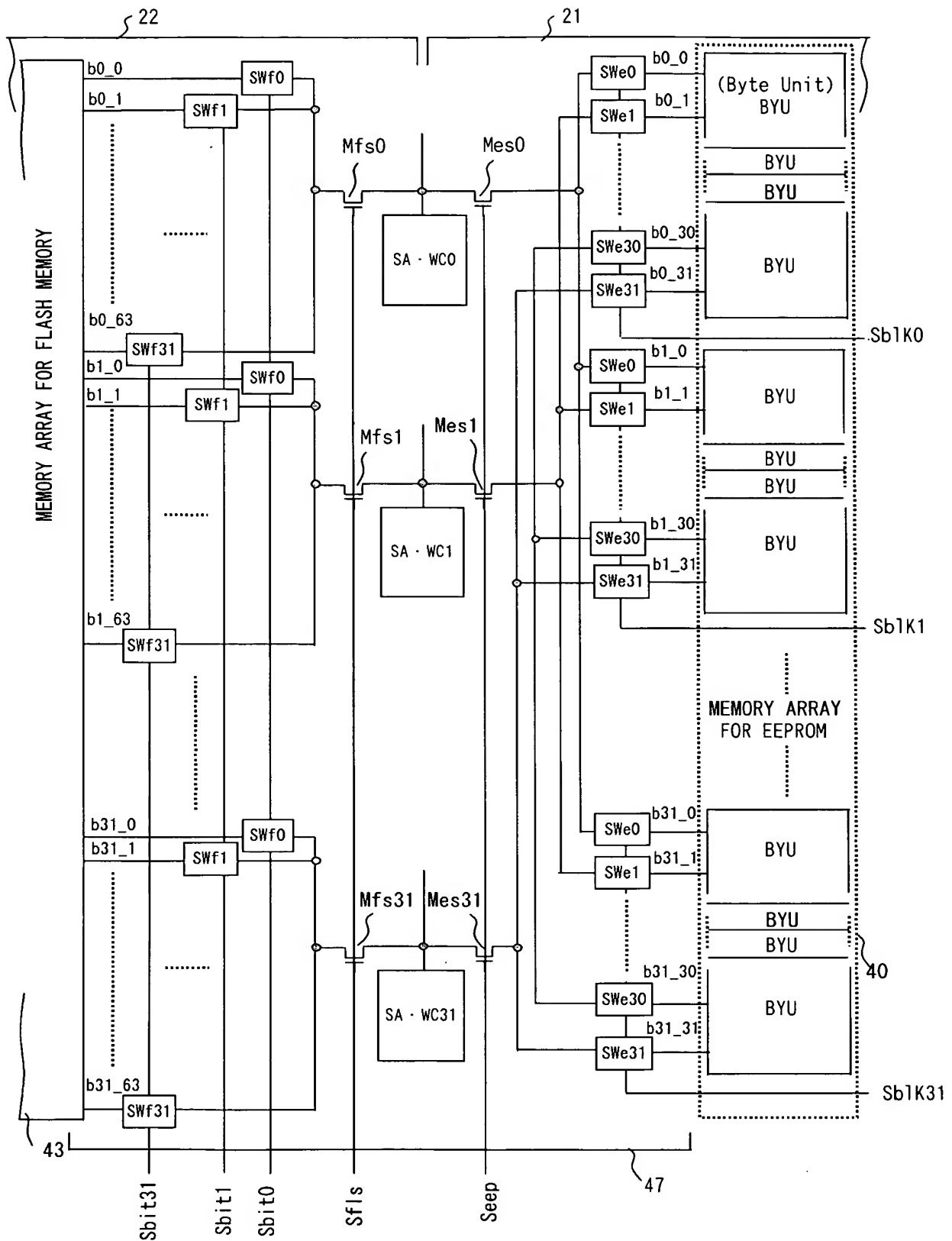


FIG. 28

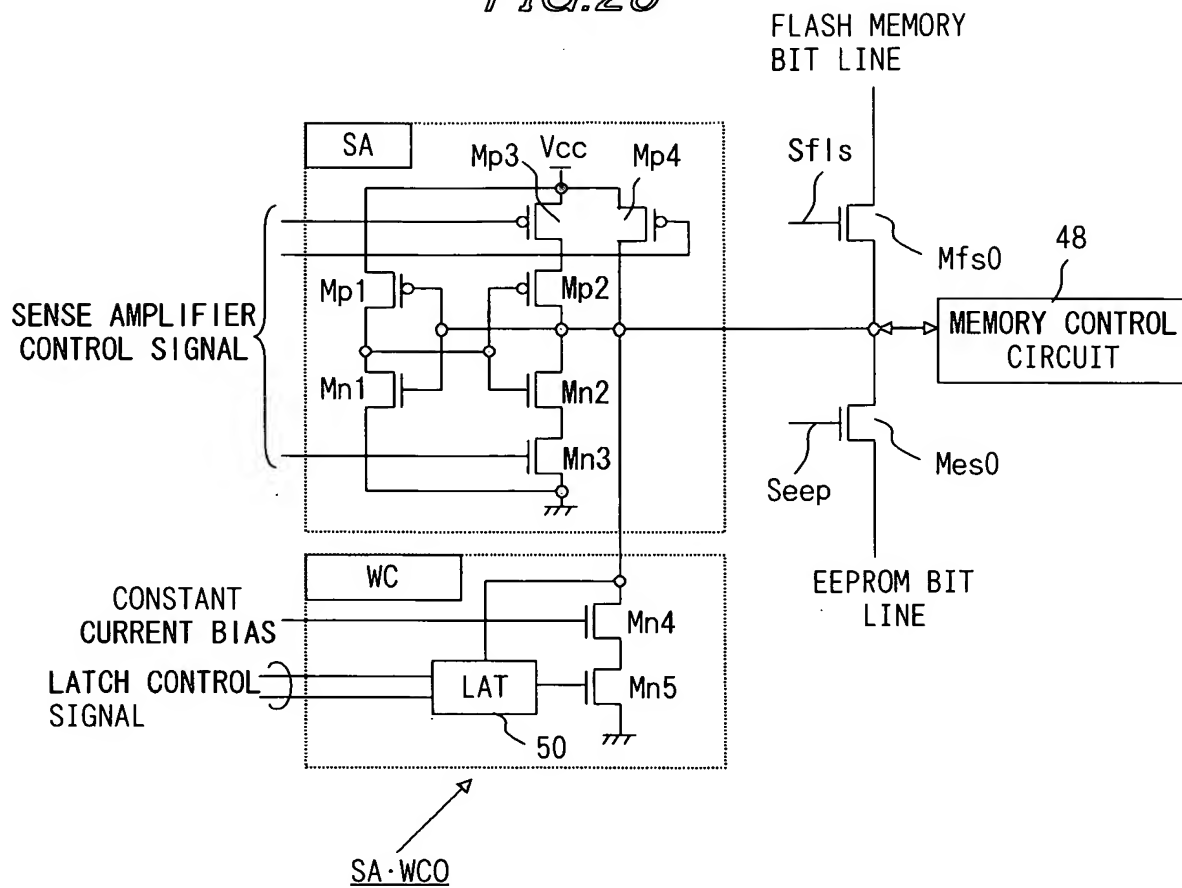


FIG. 29

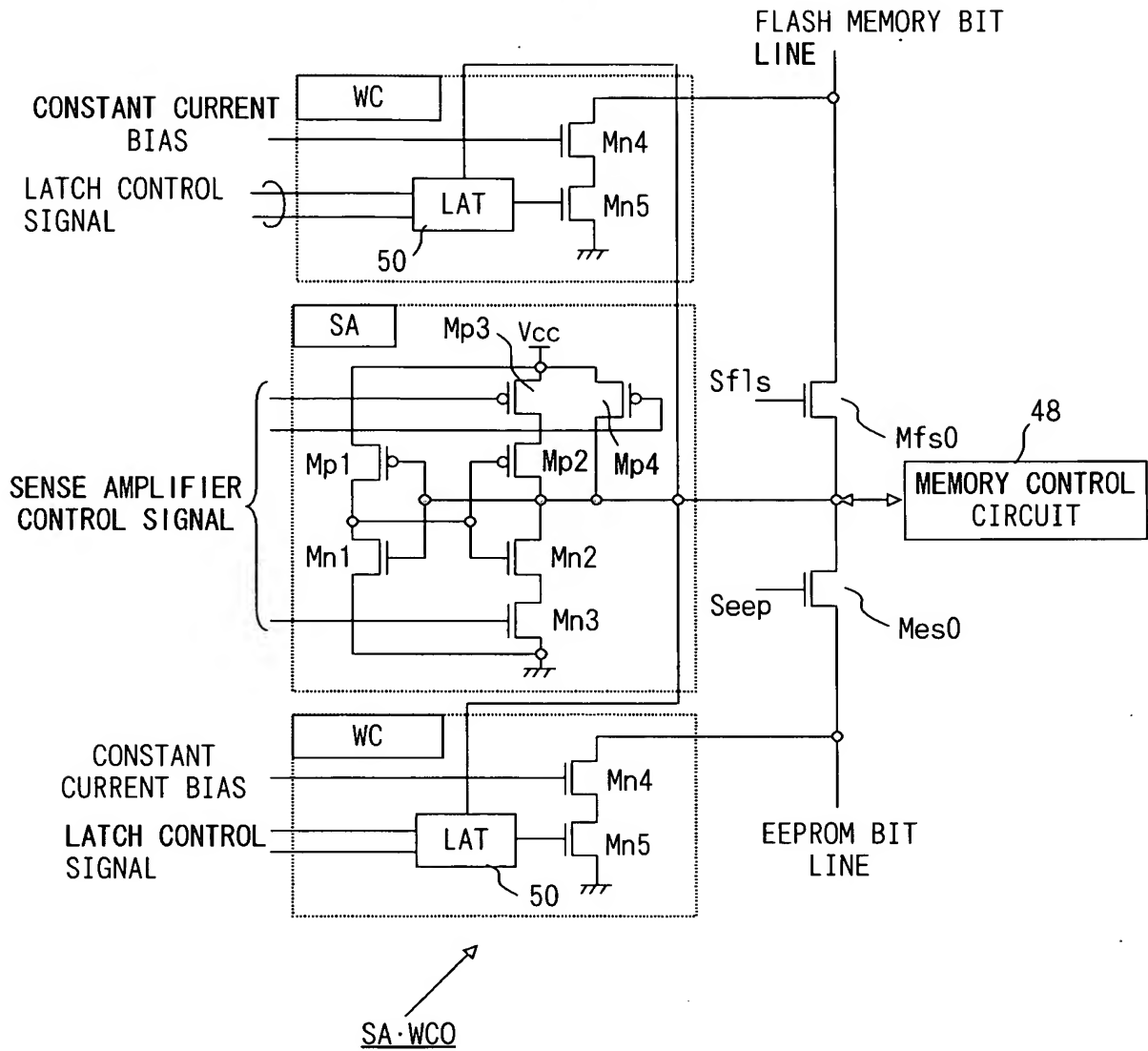


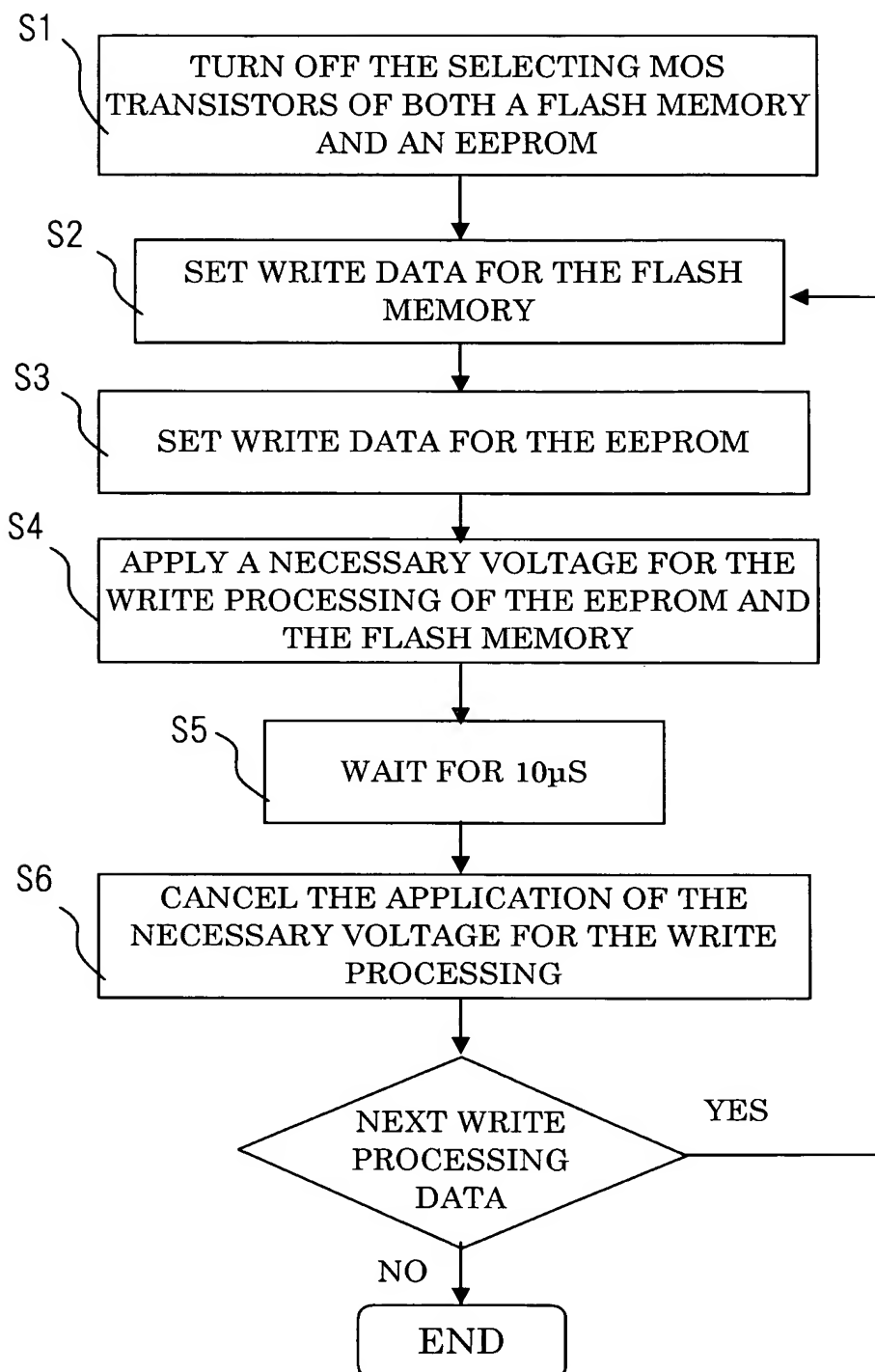
FIG.30

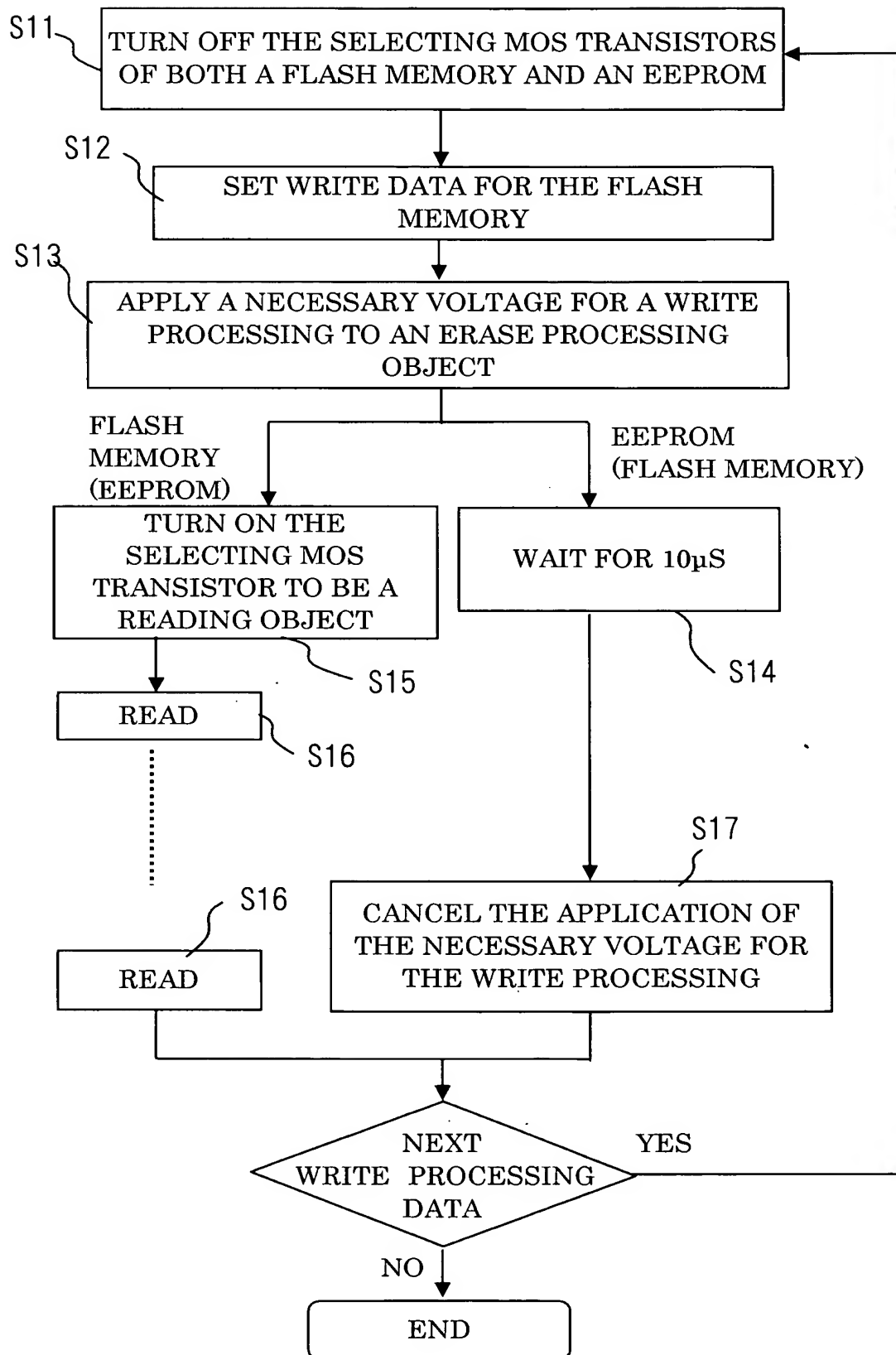
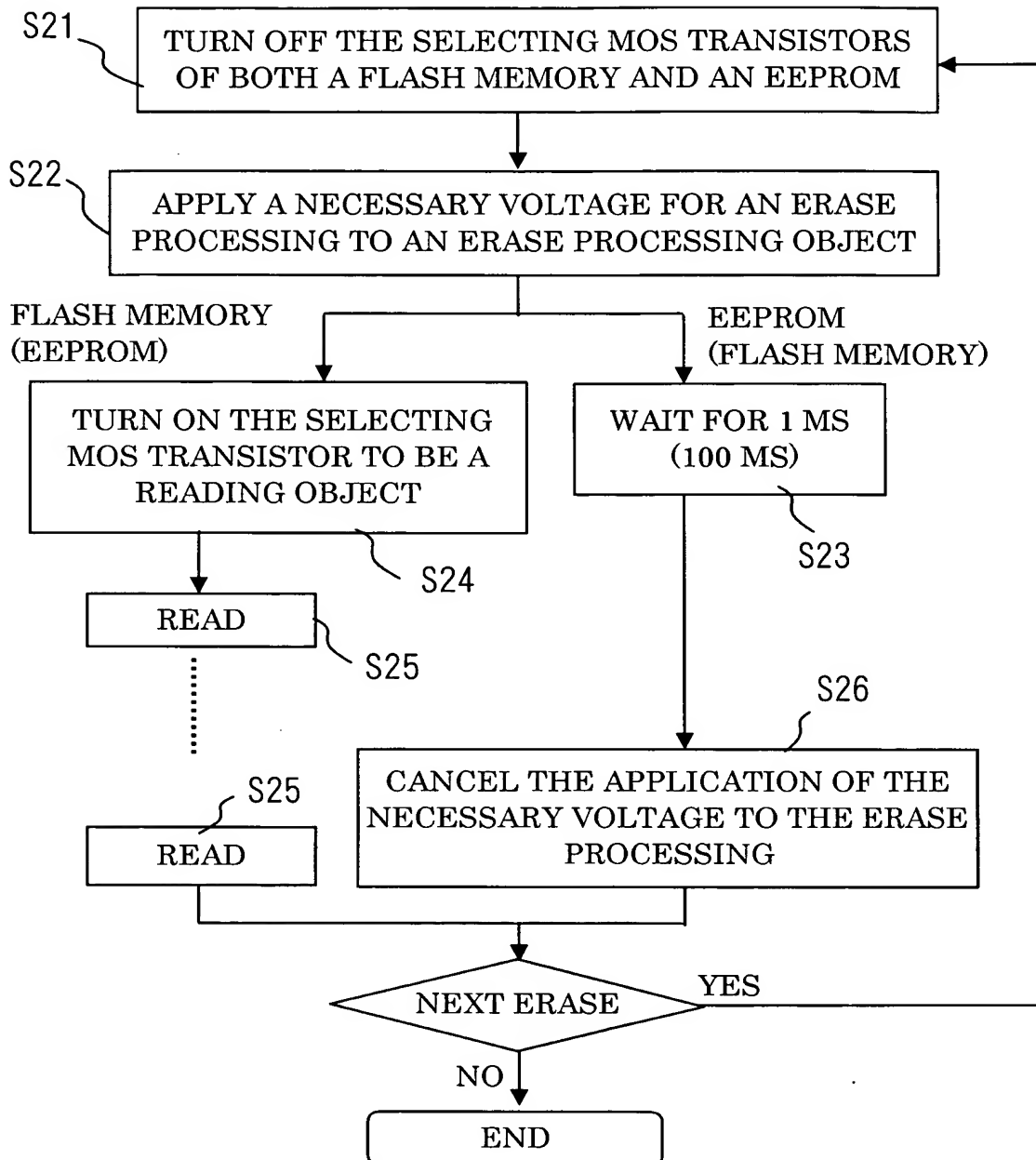
FIG.31

FIG.32**FIG.33**

	METHOD	SPECIFICATION	
		FLASH	EEPROM
ERASE PROCESSING	F-N TUNNEL	100ms	1ms
WRITE PROCESSING	HOT ELECTRON	10us/bit	10us/bit

FIG. 34

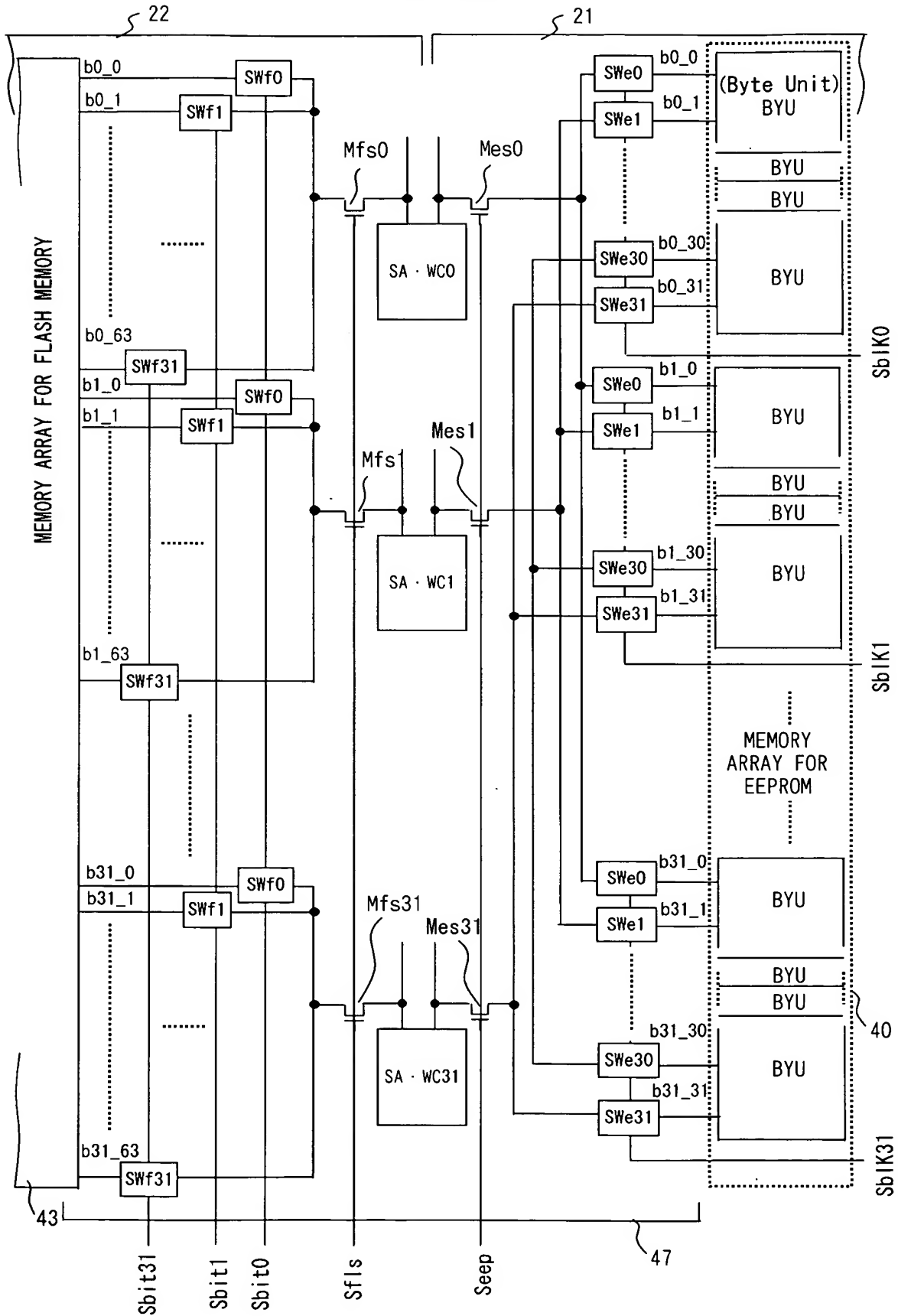


FIG. 35

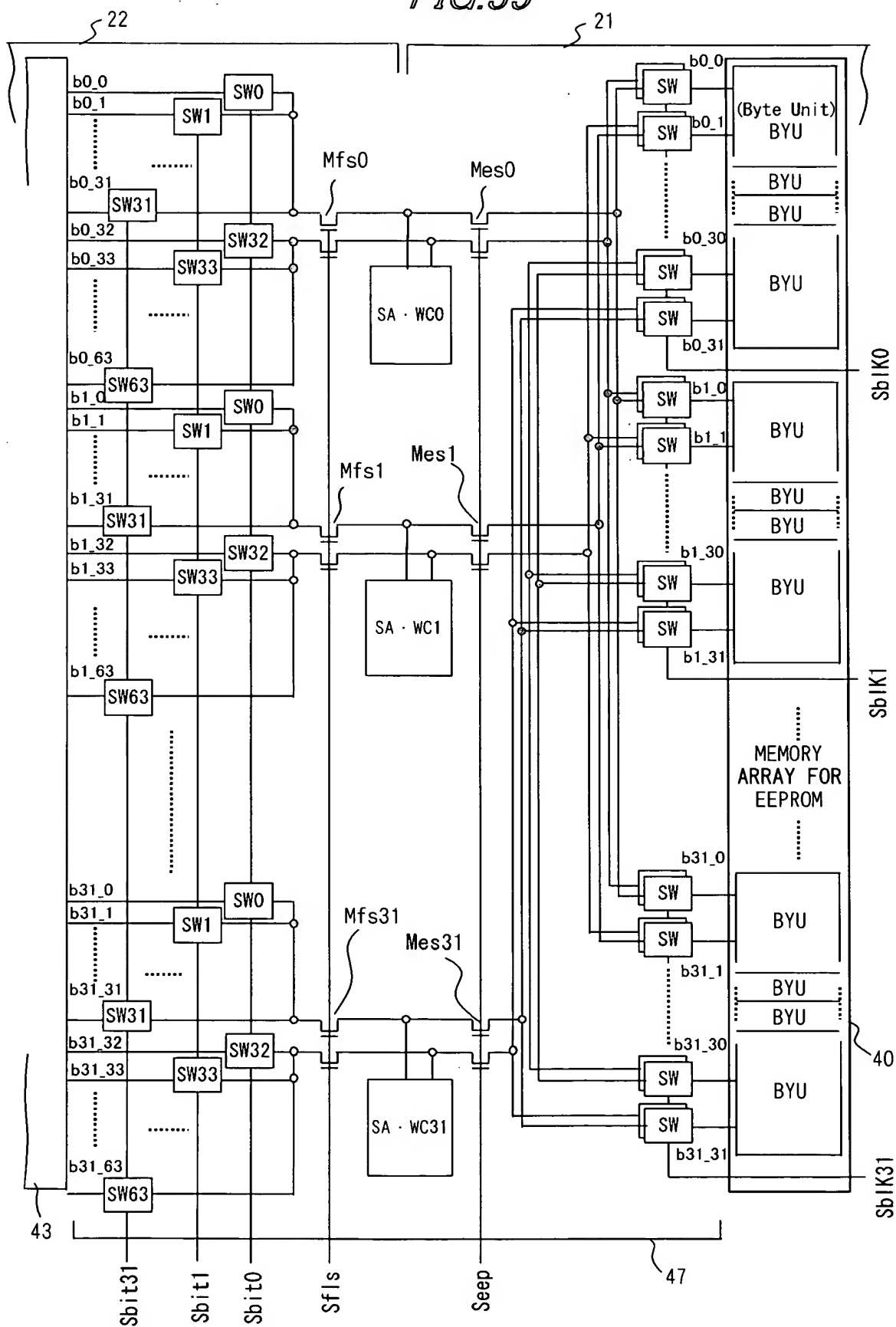




FIG. 37

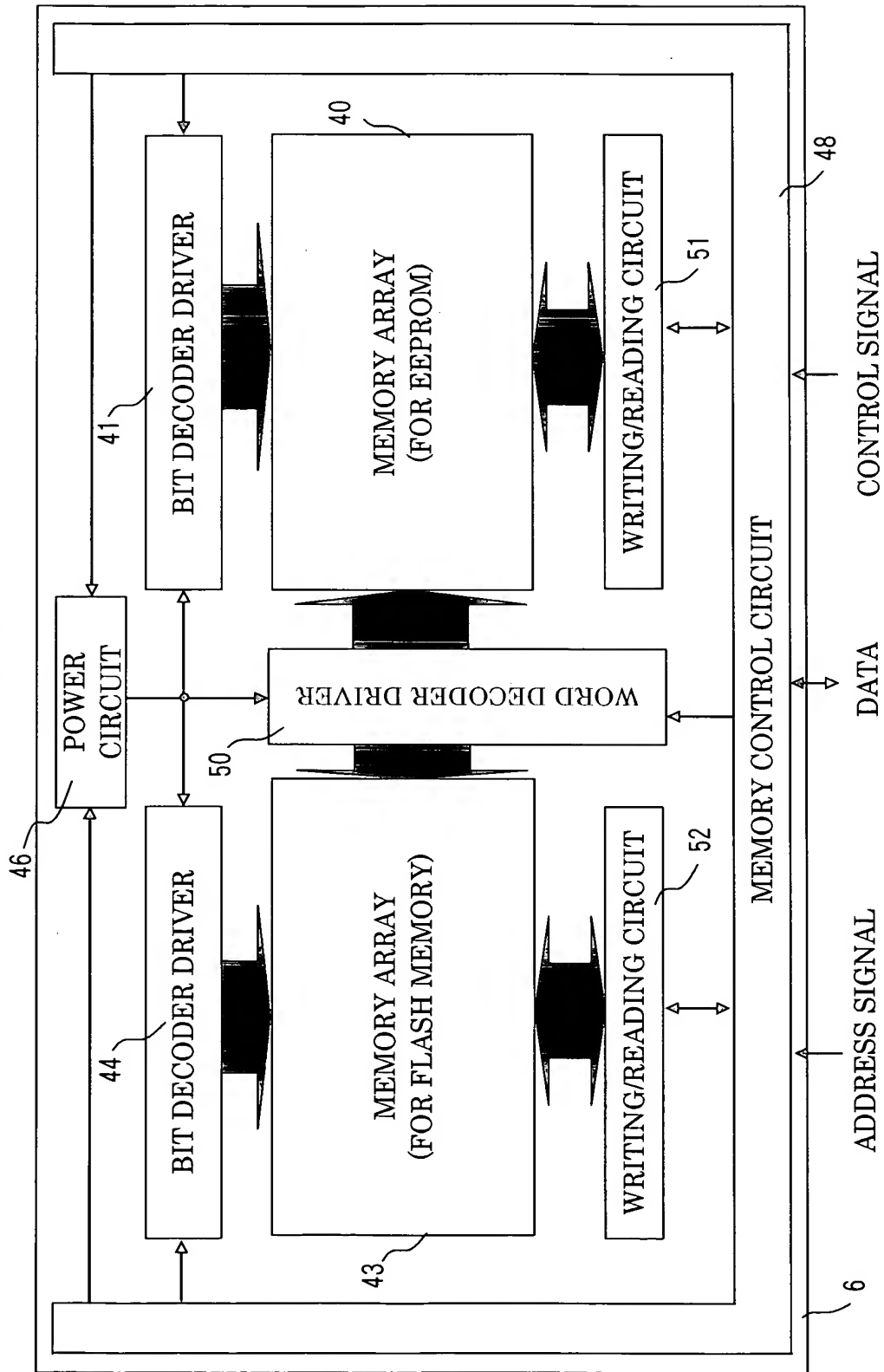


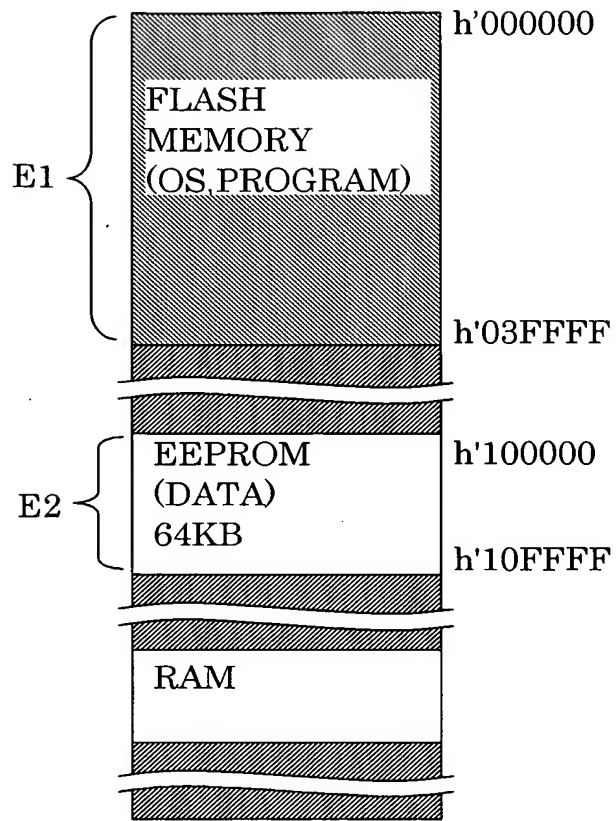
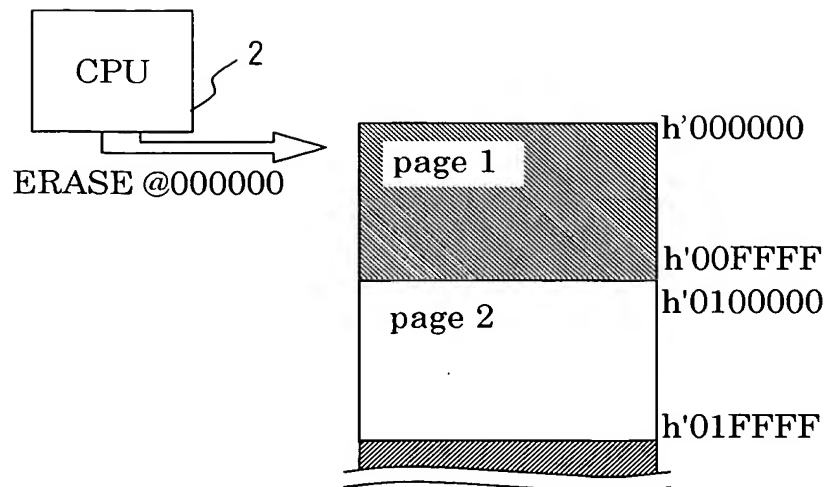
FIG.38**FIG.39**

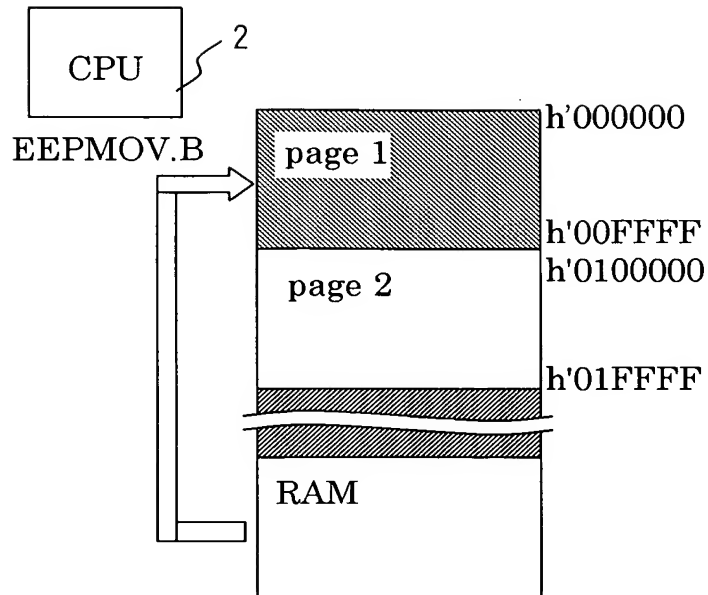
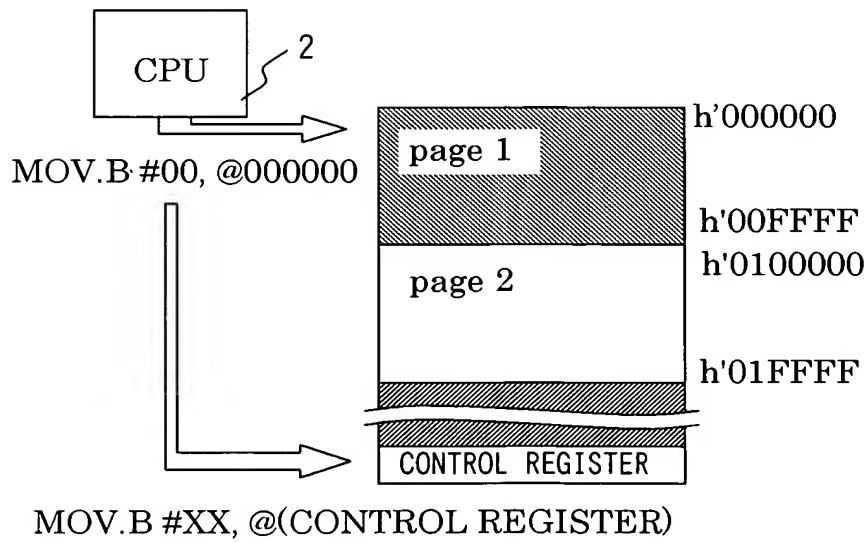
FIG.40**FIG.41**

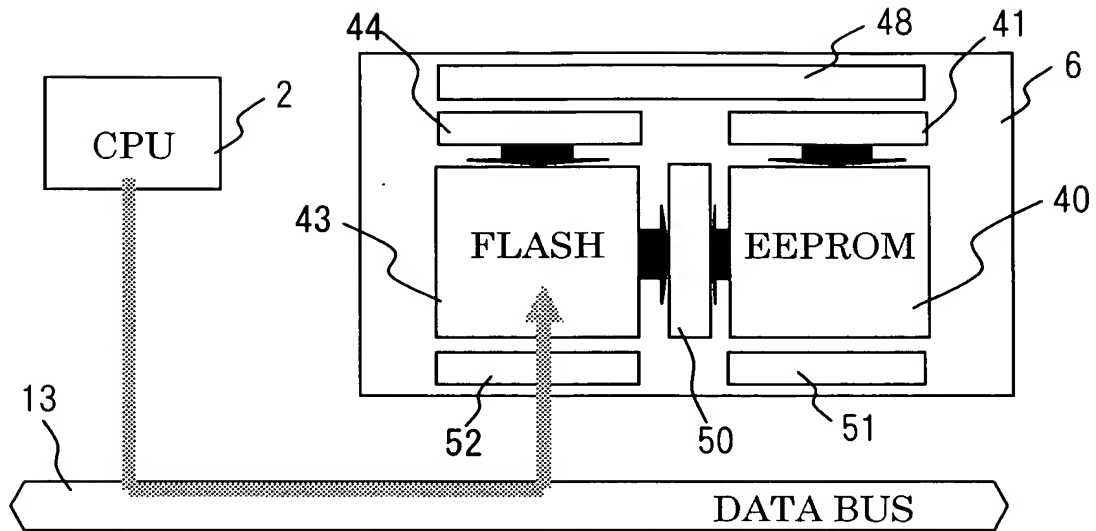
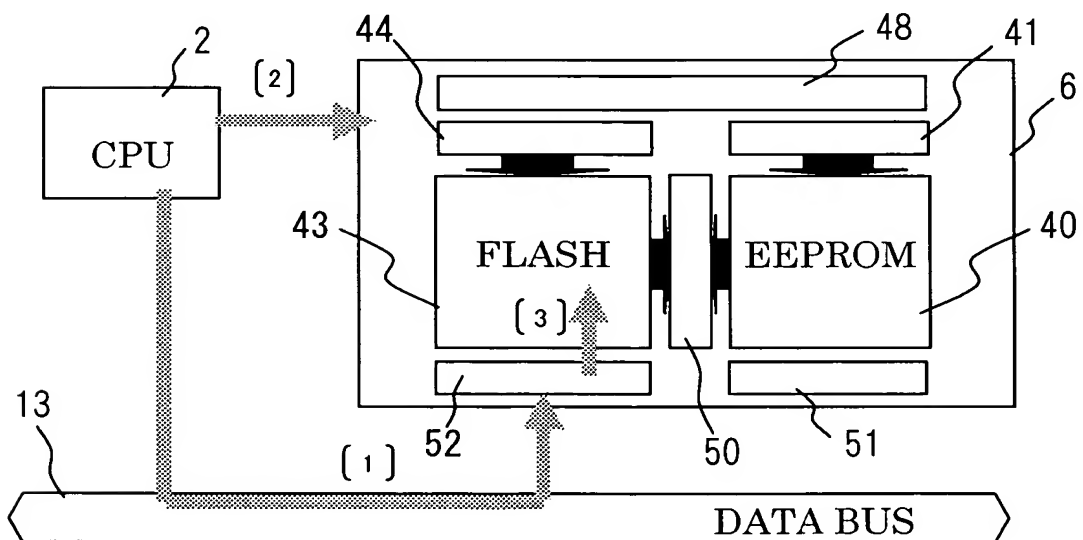
FIG. 42**FIG. 43**

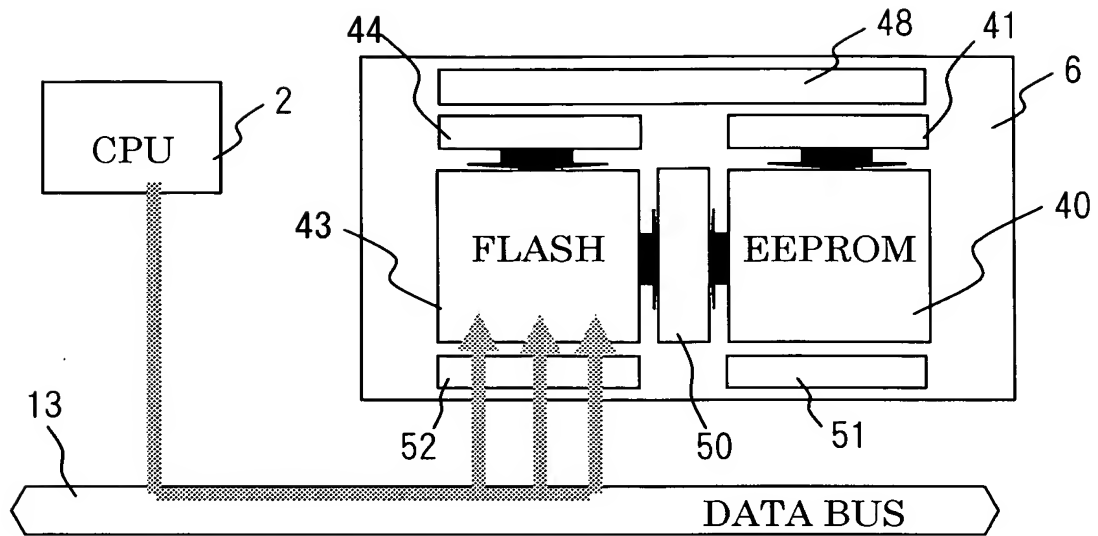
FIG. 44

FIG. 45

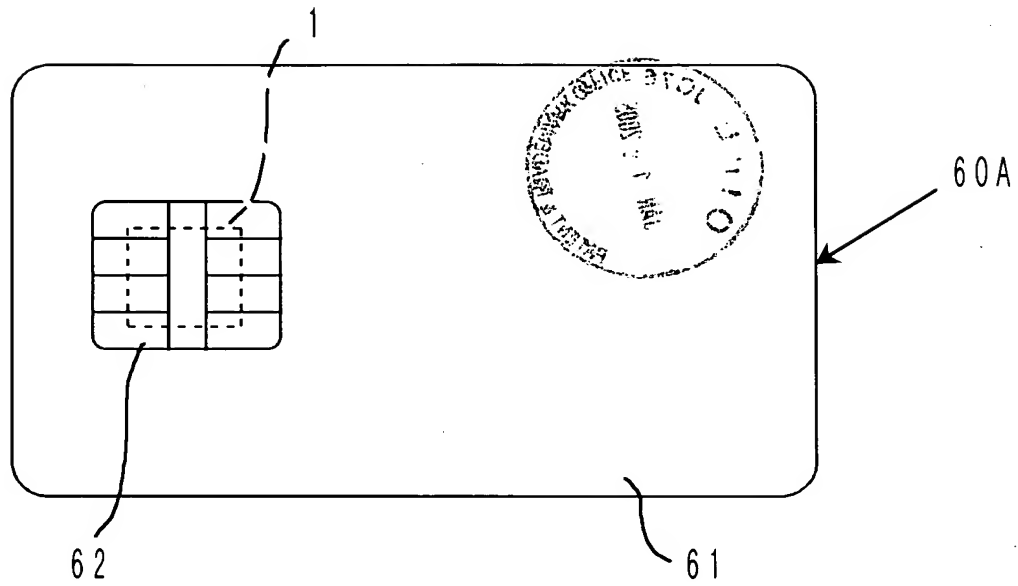
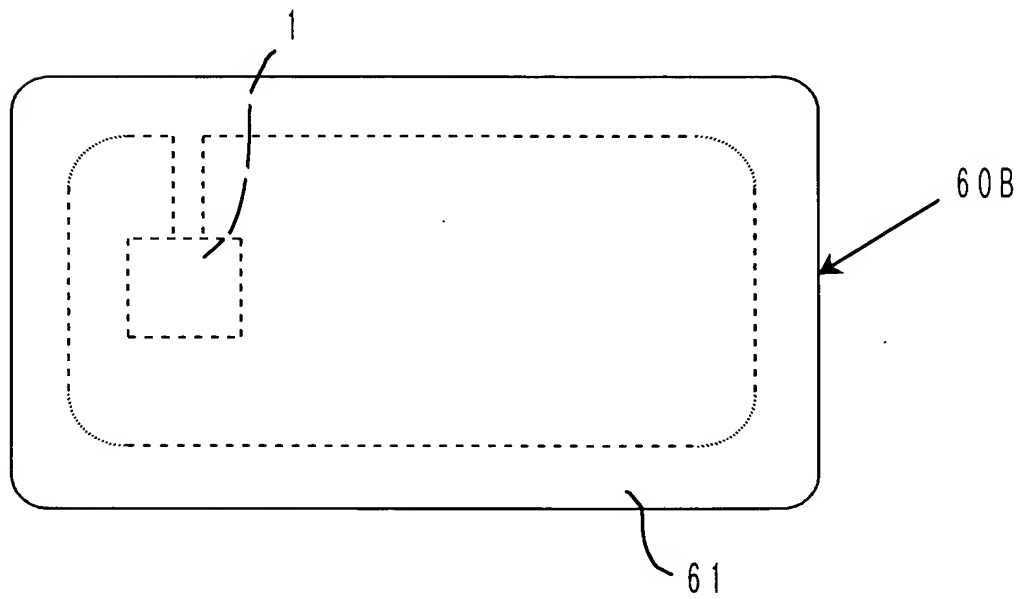


FIG. 46



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